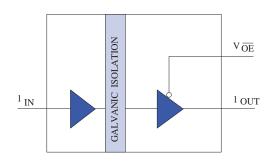


High Speed Digital Isolator for Communications Applications

Functional Diagram



Truth Table

V _I	$V_{\overline{OE}}$	Vo
L	L	L
Н	L	Н
L	Н	Z
Н	Н	Z

Features

- · +5V and +3.3V CMOS Compatible
- · 2 ns Typical Pulse Width Distortion
- · 4 ns Typical Propagation Delay Skew
- · 10 ns Typical Propagation Delay
- · High Speed: 100 MBd
- · 30 kV/µs Typical Common Mode Rejection
- · Tri State Output
- \cdot 2500V_{RMS} Isolation
- · UL1577 Approved (File # E207481)

Applications

- · Digital Fieldbus Isolation
- · Multiplexed Data Transmission
- · Computer Peripheral Interface
- · Noise Reduction in High Speed Digital Systems
- · Isolated Data Interfaces
- · Logic Level Shifting

Description

The IL710 is a CMOS digital isolator integrated with NVE's patented* IsoLoop® technology, which gives the IL710 high speed performance and excellent transient immunity specifications. The symmetric magnetic coupling barrier gives this device a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, giving the IL710 the best specifications of any isolator device. The IL710 also has a 100 Mbaud data rate, making it the world's fastest digital isolator. The IL710 is ideally suited for isolating such applications as DeviceNet/CAN, PROFIBUS, RS-485, RS422, etc. It is available in 8-pin PDIP and 8-pin SOIC packages, and is specified over the temperature range of -40°C to +100°C. Extended temperature ranges are also available. See page six for packaging and ordering information.

 $\mathit{Isoloop}^{\scriptscriptstyle{(\!0\!)}}$ is a registered trademark of NVE, Inc.

* US Patent number 5,831,426 and others

IL710 IsoLoop®

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units	
Storage Temperature	T_S	-55	175	°C	
Ambient Operating Temperature ⁽¹⁾	T_{A}	-55	125	°C	
Supply Voltage	$V_{\mathrm{DD1,}}V_{\mathrm{DD2}}$	-0.5	7	Volts	
Input Voltage	V _I	-0.5	V _{DD1} +0.5	Volts	
Input Voltage	V _{OE}	-0.5	V _{DD2} +0.5	Volts	
Output Voltage	V _O	-0.5	V _{DD2} +0.5	Volts	
Average Output Current	I _O		10	mAmps	
Lead Solder Temperature(10s)			260	°C	
ESD	2kV Human Body Model				

Insulation Specifications

Parameter	Condition	Min	Typ.	Max.	Units
Rated Voltage, 1 minute	60Hz	2500			V _{RMS}
Partial Discharge, 100% Tested	1s,5pC	2000			V _{RMS}
Creepage Distance (External)		7.036 (PDIP)			mm
		4.026 (SOIC)			
Leakage Current	240 V _{RMS}		0.1		μAmps
	60Hz				

Recommended Operating Conditions

Parameters	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	100	°C
Supply Voltage	$V_{\mathrm{DD1}}, V_{\mathrm{DD2}}$	3.0	5.5	Volts
Logic High Input Voltage	V _{IH}	$0.8V_{\mathrm{DD1}}$	V_{DD1}	Volts
Logic Low Input Voltage	V _{IL}	0	0.8	Volts
Input Signal Rise and Fall Times	$t_{\rm IR}$, $t_{\rm IF}$		1	μsec

Package Characteristics

Parameter	Symbol	Min	Typ.	Max.	Units	Test Conditions
Input-Output Momentary (5,6)	V _{ISO}	3750			V_{DC}	RH<50%, t= 1min, T _A =25C
Withstand voltage						
Capacitance (Input-Output) ⁽⁵⁾	C _{I-O}		1.1		pF	f= 1MHz
Input IC Junction-to-Case (PDIP)	$\theta_{ m JCT}$		150		°C/W	Thermocouple located at
Thermal Resistance (SOIC)	$\theta_{ m JCT}$		240		°C/W	center underside of package
Package Power Dissipation	P_{PD}			150	mW	

Electrical Specifications

Electrical Specifications are $T_{\mbox{\scriptsize min}}$ to $T_{\mbox{\scriptsize max}}$ unless otherwise stated.

Parameter	Symbol		Iin	Т	Тур.		Max		Test Conditions
DC Specifications		3.3V	5V	3.3V	5V	3.3V	5V		
Input Quiescent Supply Current	I_{DD1}						10	μΑ	
Output Quiescent Supply Current	I_{DD2}			2.2	4.0	3.3	5	mA	
Logic Input Current	I _I	-10	0			1	0	μΑ	
Logic High Output Voltage	V _{OH}	V_{DD2}	-0.1	V _{DI}	D2			V	$I_{O} = -20 \mu A, V_{I} = V_{IH}$
		0.8*V	DD2	V_{DD2}	-0.5			,	$I_O = -4 \text{ mA}, V_I = V_{IH}$
Logic Low Output Voltage	V _{OL}			0	1	0.	1	V	$I_0 = 20 \mu\text{A}, V_I = V_{II}$
				0.	5	0.	8	•	$I_O = 4 \text{ mA}, V_I = V_{IL}$
Switching Specifications at 25°C									
Clock Frequency fmax						50	50	MHz	$C_L = 15 \text{ pF}$
Data Rate						100	100	MBd	$C_L = 15 \text{ pF}$
Pulse Width	PW	10	10					ns	
Propagation Delay Input to Output (High to Low)	t _{PHL}			12	10	18	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Input to Output (Low to High)	t _{PLH}			12	10	18	15	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High to High Impedance)	t _{PHZ}			3	3	5	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (Low to High Impedance)	t _{PLZ}			3	3	5	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to High)	t _{PZH}			3	3	5	5	ns	$C_L = 15 \text{ pF}$
Propagation Delay Enable to Output (High Impedance to Low)	t _{PZL}			3	3	5	5	ns	$C_L = 15 \text{ pF}$
Pulse Width Distortion ⁽²⁾ tPHL- tPLH	PWD			2	2	3	3	ns	$C_L = 15 \text{ pF}$
Propagation Delay Skew ⁽³⁾	t _{PSK}			4	4	6	6	ns	$C_L = 15 \text{ pF}$
Output Rise Time (10-90%)	t _R			2	1	4	3	ns	$C_L = 15 \text{ pF}$
Output Fall Time (10-90%)	t _F			2	1	4	3	ns	$C_L = 15 \text{ pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) (4)	CMH CML	20	20	30	30			kV/μs	Vcm = 300V

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

IL710 IsoLoop®

Notes:

- Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
- 2. PWD is defined as $|t_{PHL} t_{PLH}|$. %PWD is equal to the PWD divided by the pulse width.
- 3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
- 4. $\rm CM_H$ is the maximum common mode voltage slew rate that can be sustained while maintaining Vo > 0.8 V_{DD2}. $\rm CM_L$ is the maximum common mode input voltage that can be sustained while maintaining Vo < 0.8 V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
- 5. Device is considered a two terminal device: pins 1-4 shorted and pins 5-8 shorted.
- Input Output Momentary Withstand Voltage is a dielectric voltage and should not be interpreted as an input - output continuous voltage.

Application Notes:

Power Consumption

The IL710 achieves its low power consumption from the manner by which it transmits data across its isolation barrier. By detecting the edge transitions of the input logic signal and converting this to a narrow current pulse which drives the isolation barrier, the isolator then latches the input logic state in the output latch. Since the current pulses are narrow, about 2.5 ns wide, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers whose power consumption is heavily dependent on its on state and frequency. The static power consumption for the IL710 in either state approaches the CMOS quiescent value.

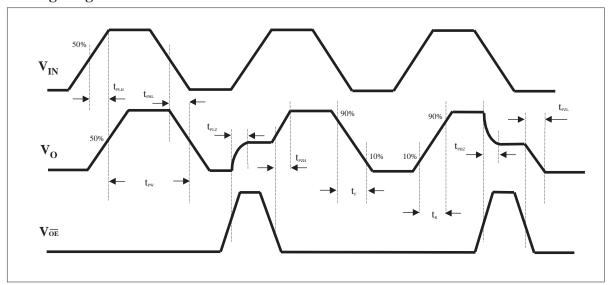
Power Supplies

It is recommended that low ESR ceramic capacitors be used to decouple the supplies. 10nF capacitors should be placed as close to the device as possible between V_{DD1} and GND_1 , as well as between V_{DD2} and GND_2 .

Signal Status on Start-up and Shut Down

To minimize power dissipation, the input signal to the IL710 is differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider the inclusion of an initialization signal in his start-up circuit.

Timing Diagram

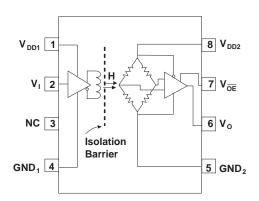


Legend

t _{PLH}	Propagation Delay, Low to High
t _{PHI}	Propagation Delay, High to Low
t _{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low to High Impedance
t _{PZH}	Propagation Delay, High Impedance to High
t _{PHZ}	Propagation Delay, High to High Impedance
t _{PZI}	Propagation Delay, High Impedance to Low
t _R	Rise Time
t _E	Fall Time

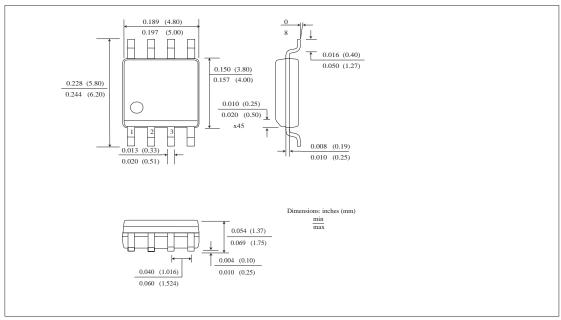
Pin Connections

1	V_{DD1}	Input Power Supply
1	V DD1	1 11 0
2	V_{I}	Logic Input Signal
3	NC	No Internal Connection
4	GND_1	Input Power Supply Ground
5	GND_2	Output Power Supply Ground
6	V_{o}	Output Logic Signal
7	$V_{\overline{ ext{OE}}}$	Logic Output Enable
8	V_{DD2}	Output Power Supply

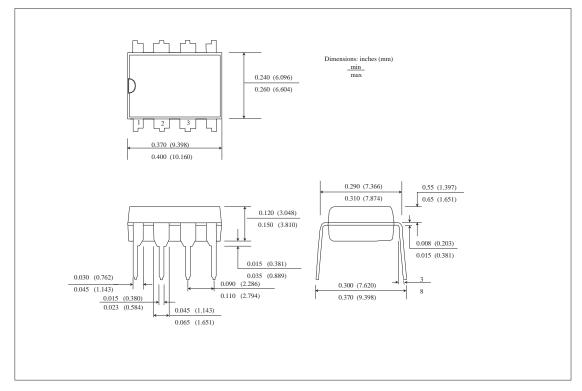


IL710 IsoLoop®

IL710-3 (Small Outline SOIC-8 package)



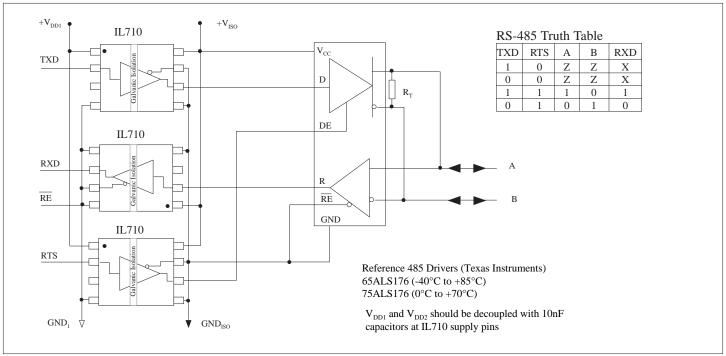
IL710-2 (8-Pin PDIP Package)



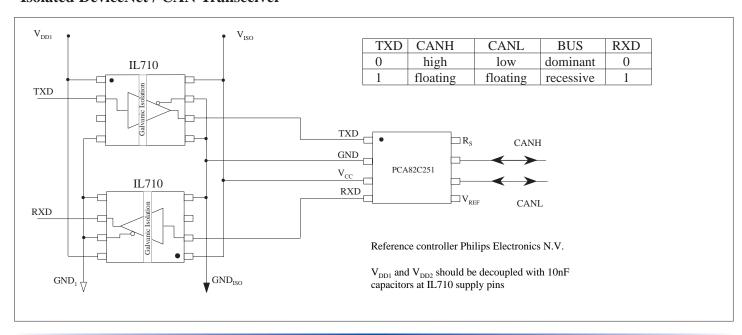
Ordering Information: Order parts per the above numbers.

Applications

Isolated PROFIBUS / RS-485



Isolated DeviceNet / CAN Transceiver



About NVE

An ISO 9001 Certified Company

NVE Corporation is a high technology components manufacturer having the unique capability to combine leading edge Giant Magnetoresistive (GMR) materials with integrated circuits to make novel electronic components. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometer), Digital Magnetic Field Sensors, Digital Signal Isolators and Isolated Bus Transceivers.

NVE is a leader in GMR research and in 1994 introduced the world's first products using GMR material, a line of GMR magnetic field sensors that can be used for position, magnetic media, wheel speed and current sensing.

NVE is located in Eden Prairie, Minnesota, a suburb of Minneapolis. Please visit our Web site at www.nve.com or call 952-829-9217 for information on products, sales or distribution.

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Specifications shown are subject to change without notice.

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